forming a conductive line, which is to be connected to the conductive region, on the first interlayer dielectric layer;

forming a second interlayer dielectric layer on the conductive line;

removing portions of the first interlayer dielectric layer, conductive line, and second interlayer dielectric layer which overlie the conductive region to form a contact hole which exposes the conductive region; and

filling the contact hole with a conductive material to connect the conductive line to the conductive region,

wherein said removing of portions of the first interlayer dielectric layer, conductive line, and second interlayer dielectric layer comprises:

forming a patterned photosensitive film on the second interlayer dielectric layer, the patterned photosensitive film defining an opening therein having a width that is greater than the width of the conductive line,

etching the second interlayer dielectric layer using the photosensitive film pattern as an etch mask until the conductive line is exposed, and

etching the conductive line and the first interlayer dielectric layer using the etched second interlayer dielectric layer as an etch mask.

8. (Amended) A method of fabricating a semiconductor device, comprising:

forming a conductive region at the top of a semiconductor substrate;

forming a first interlayer dielectric layer on the semiconductor substrate over the entirety of the conductive region;

forming a conductive line, which is to be connected to the conductive region, on the first interlayer dielectric layer;

forming a second interlayer dielectric layer on the conductive line;

removing portions of the first interlayer dielectric layer, conductive line, and second interlayer dielectric layer which overlie the conductive region to form a contact hole which exposes the conductive region; and

filling the contact hole with a conductive material to connect the conductive line to the conductive region,

wherein the forming of the conductive line comprises:

forming a dielectric film pattern defining a line-shaped opening on the first interlayer dielectric layer, and

depositing conductive material in the line-shaped opening.

Please cancel claim 1.

REMARKS

Applicants gratefully acknowledge that the Examiner has allowed claims 9, 10, 14, 15 and 21-23.

Applicants have amended claims 2 and 8 and canceled claim 1. Accordingly, claims 2-10, 14, 15 and 21-23 remain pending in the application.

Reexamination and reconsideration of the present application are requested in view of the following remarks.